IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

JAE-BON KOO *et al.*

Serial No.:	10/764,525	Examiner:	LUKE, DANIEL M.
Filed:	27 January 2004	Art Unit:	2813

For: FLAT PANEL DISPLAY WITH ANODE ELECTRODE LAYER AS POWER SUPPLY LAYER AND FABRICATION METHOD THEREOF

INFORMATION DISCLOSURE STATEMENT

Mail Stop
Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97 and 1.98 as amended, Applicant cites, describes, and provides copies of the following art references. Under 37 C.F.R. §1.98(a)(2) however, copies of U.S. patent reference(s) are not provided.

Foreign Patent Reference(s)

1. Japanese Patent Publication No. 2003-15548 to Kimura et al., entitled *METHOD FOR MANUFACTURING ORGANIC EL DISPLAY BODY, METHOD FOR ARRANGING SEMICONDUCTOR DEVICE, METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE, METHOD FOR MANUFACTURING OPTOELECTRONIC DEVICE, OPTOELECTRONIC DEVICE, AND ELECTRONIC EQUIPMENT*, published on 17 January 2003 (*previously cited in Applicant's IDS filed on 13 October 2006*);
2. Japanese Patent Publication No. 2001-134214 to Furumiya et al., entitled *DISPLAY*

DEVICE, published on 8 May 2002 (*previously cited in Applicant's IDS filed on 29 June 2007*);

3. Japanese Patent Publication No. 09-160509 to Sakamoto, entitled *ACTIVE-MATRIX SUBSTRATE AND ITS MANUFACTURE*, published on 20 June 1997 (*with English abstract*);
4. Japanese Patent Publication No. 11-126691 to Kusaka, entitled *ORGANIC EL ELEMENT AND ITS MANUFACTURE*, published on 11 May 1999 (*with English abstract*);
5. Japanese Patent Publication No. 2002-32037 to Koyama et al., entitled *DISPLAY DEVICE*, published on 31 January 2002 (*with English abstract*);
6. Japanese Patent Publication No. 2003-17273 to Nakayama, entitled *DISPLAY DEVICE AND ITS MANUFACTURING METHOD*, published on 17 January 2003 (*with English abstract*);

Other Documents

- Japanese Office action in the Japanese patent application No. 2003-354515, mailed 15 April 2008.

DISCUSSION

Sakamato JP'509, according to the Japanese Office action in the Japanese patent application No. 2003-354515 (mailed 15 April 2008), discloses that a gate electrode 1, a scanning line 3, and part 14 of a signal line 2 are formed on a glass substrate 20 as films continuing to a gate insulating film 4 and an undoped a-Si film 5. Next, a channel protection film 11 is laminated, a contact hole 8 is patterned in a drain 6 and a source 7, and at the same time, contact parts around the extensions of the scanning line 3 and of the signal line 2 and a contact hole 9 with the signal line 2 are formed to form a contact layer 10. Then, a conductive material is deposited and a picture element electrode 15, a source electrode 13 and a drain electrode 12, and a part 14 of the signal line 2 are patterned.

Kusaka JP'691 discloses that when a transparent electrode (an ITO thin film) 4 is formed on an organic thin film 3, a cooled metal mask is placed in sputtered particle flow, and the temperature increase of the organic thin film caused by unnecessary particles is prevented. The energy of the sputtered particles passed through holes of the mask and reached to the surface of a substrate 1 is suppressed to the minimum level, part of the particles are ionized, energy is supplemented by field acceleration, and thereby stable film formation is realized.

Koyama et al. JP'037 discloses plural pieces of draw-out ports of power source supplying lines which are arranged in this display device. The potential of the wiring resistance between an external input terminal and the power source supplying line of a pixel part is compensated by supplying a potential to the power source supplying line with a feedback amplifier. Moreover, power source supplying lines are arranged in a matrix shape in addition to the constitution.

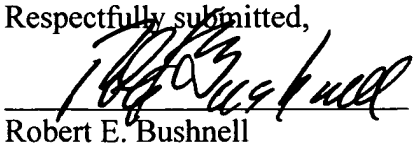
Nakayama JP'273 discloses the display device comprising a first electrode 201 made of a light reflecting material, a second electrode 108 made of a light transmission material, and an organic EL layer 107 that is pinched by these first electrode 201 and second electrode 108. A reflecting wall 202 for reflecting the emitting- light h emitted in the organic EL layer 107 toward the second electrode 201 side is provided in the surroundings of the organic EL layer 107. This reflecting wall 202 is constructed as an inner circumference wall formed in a concave shape of the first electrode 201.

Pursuant to 37 CFR §1.97(d), the undersigned attorney hereby certifies that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign patent application not more than three (3) months prior to the filing of the statement.

The citation of the foregoing references is not intended to constitute an assertion that other or more relevant art does not exist. Accordingly, the Examiner is requested to make a wide-ranging and thorough search of the relevant art.

No fee is incurred by this Statement.

Respectfully submitted,



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